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(54) Non-volatile semiconductor memory device using a differential cell in a memory cell

Eine nichtflüchtige Halbleiterspeicheranordnung, die eine differentielle Zelle als Speicherzelle gebraucht

Dispositif de mémoire à semiconducteurs non volatile utilisant une cellule différentielle de cellule de mémoire

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(56) References cited:
EP-A- 0 337 393
EP-A- 0 396 263

EP 0 506 989 B1

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Description

The present invention relates to a non-volatile semiconductor memory device using a non-volatile transistor in a memory cell.

In a non-volatile semiconductor memory such as an EPROM (erasable programmable read only memory), a memory cell conventionally consists of one transistor, and "1" or "0" level of data is determined by turning on or off a selected memory.

In recent years, a high-speed operation of a semiconductor memory has been required as the processing speed of a CPU is increased. In accordance with this, conventionally, several types of EPROMs capable of performing high-speed operations are disclosed in some literatures. For example, "A 25ns 16K CMOS PROM using a 4-Transistor Cell" is described in the "ISSCC, DIGEST OF TECHNICAL PAPERS" in pp. 162 - 163 published in the United States on Feb., 1985, "A 23ns 256K EPROM with Double-Layer Metal and Address Transition Detection" is described in the ISSCC, DIGEST OF TECHNICAL PAPERS" in pp. 130 - 131 published in the United States on Feb., 1985, and "16ns CMOS EPROM" is issued in the subcommittee of the Institute of Electrical and Electronics Engineers of Japan, 1989.

Memory cells known as differential cells are applied to the EPROMs described in the above literatures. In the differential cell, a memory cell consists of at least two transistors. In a data write mode, the two transistors are set in two different states such as high and low states of a threshold voltage depending on an injection state of electrons. In a data read mode, readout potentials from the two transistors are compared by a sense amplifier to read out data.

The differential cell has a larger noise margin than that of a general conventional memory cell consisting of one transistor and operated such that a readout potential from a cell transistor is compared with an intermediate level serving as a reference potential. Therefore, the differential cell is advantageously suitable for a high-speed operation.

A pattern layout of the differential cell will be described below. Conventionally, the differential cell has a layout in which two transistors are arranged to be adjacent to each other.

Fig. 1 is a circuit diagram showing a read circuit of a conventional EPROM having a differential cell. As shown in Fig. 1, conventionally, a pair of bit lines BL and $\overline{BL}$ selected by two column selecting transistors 1-1 and 1-2 are arranged to be adjacent to each other. A plurality of bit lines BL are commonly connected to a transistor 2-1 serving as a transfer gate, and a plurality of bit lines $\overline{BL}$ having the same number as that of the bit lines BL are commonly connected to a pass transistor 2-2 serving as a transfer gate. The pass transistors 2-1 and 2-2 are connected to a sense amplifier 3. In the sense amplifier 3, the potentials of a pair of bit lines BL and $\overline{BL}$ selected by the column selecting transistors 31-1 and 31-2 are applied, and the potentials are compared with each other to detect readout data from a memory cell (not shown).

In the EPROM with the above arrangement, one memory cell consists of two transistors for respectively storing different signal levels, and the two transistors are arranged to be adjacent to each other. According to this pattern layout, the following problem is posed.

In Fig. 1, column selecting transistors 1-1 and 1-2 are difficult to be arranged. The size of a memory cell is minimized, and a pitch in a column direction has a minimum size. In this state, since two bit lines BL and $\overline{BL}$ must be parallelly arranged in a direction perpendicular to the column direction, it is very difficult to arrange the bit lines. In addition, even if the bit lines can be arranged as a pattern, since portions 4 where the bit lines cross each other are formed and one of two bit lines must be jumped over the other by using another wiring means such as a diffusion layer, the wiring pattern is complicated. Furthermore, since the wiring resistances of the bit lines are different from each other symmetry of the column selecting transistors is degraded.

With the above arrangement, symmetry of the differential cell is degraded. For example, a differential cell shown in Fig. 2A is known as an interleaved cell, and the interleaved cell consists of two staggered non-volatile transistors. Fig. 2B is an equivalent circuit diagram of Fig. 2A. In the memory cell in Fig. 2B, word lines WL are arranged to cross bit lines BL and $\overline{BL}$. Since different signal levels must be read out from a pair of transistors to the pair of bit lines, one word line WL is commonly used for a pair of transistors MR and $\overline{MR}$ which are obliquely adjacent to each other through a source line SL in Fig. 2B.

In general, impurity ions are implanted in the channel regions of two transistors constituting a memory cell to control a threshold voltage, and a predetermined angle is given to the implantation direction upon the ion implantation to form a shallow channel region having good characteristics. For this reason, in an interleaved cell, since directions of implantation in the channel regions of two transistors constituting a 1-bit memory cell are different from each other when the directions are viewed from the sources of the two transistors, the transistors MR and $\overline{MR}$, characteristics of which are preferably equal to each other, become different from each other in characteristics.

Since source lines wired to be in contact with the source regions are every several bit lines BL and BL alternately arranged, the positions of the source lines and the corresponding pair of transistors are not symmetrical. This arrangement is formed not only in the interleaved cell but in all differential cells in which bit lines BL and $\overline{BL}$ are alternately arranged.

As described above, in a conventional non-volatile semiconductor memory device, two transistors constituting a 1-bit memory cell are arranged to be adjacent

to each other. Therefore, since a pair of bit lines must be alternately arranged, column selecting transistors are difficult to be arranged, characteristics of two transistors constituting the memory cell are disadvantageously different from each other.

EP-A-0 337 393 shows an EPROM in which for each memory bit, complementary data is programmed in a pair of cells. The pair of cells are arranged at a corresponding place in two matrices. There is no suggestion of the feature of the present invention of a memory cell comprising differential cells.

It is, therefore, an object of the present invention to provide a non-volatile semiconductor memory device having a layout in which the pattern layout of a column selecting transistor is simplified and the characteristics of two transistors constituting a memory cell are equal to each other.

According to the present invention, there is provided a non-volatile semiconductor memory device as set out in claim 1. Preferred features are set out in the dependent claims.

According to the arrangement of the present invention, the two transistors constituting a 1-bit memory cell are respectively formed in different memory cell arrays, and the memory cell arrays, column selecting transistors, or the like can be patterned to be symmetrical.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a circuit diagram showing an arrangement of a read circuit of a conventional EPROM using differential cells;

Fig. 2A is a plan view of a pattern showing memory cells of the conventional EPROM using differential cells;

Fig. 2B is an equivalent circuit diagram showing the conventional EPROM in Fig. 2A;

Fig. 3 is a circuit diagram showing an arrangement according to an embodiment of the present invention.

Fig. 4 is a plan view of a pattern showing an arrangement of a column selector section in the circuit in Fig. 3;

Figs. 5 and 6 are plan views showing arrangements of an memory cell array section of the circuit in Fig. 3; and

Fig. 7 is a circuit diagram showing an arrangement according to a modification of the present invention.

An embodiment of the present invention will be described below with reference to the accompanying drawings.

Fig. 3 is a circuit diagram showing an arrangement of a read circuit when the present invention is applied to an EPROM. A plurality of differential cells each consisting of first and second non-volatile transistors for storing 1-bit data are formed in memory cell arrays 11-1 and 11-2, and a pair of cells are respectively formed in the different memory cell arrays. That is, the first non-volatile transistors constituting the differential cells are formed in the memory cell array 1-1, and the second non-volatile transistors constituting the differential cells are formed in the memory cell array 1-2.

The transistors formed in the memory cell array 11-1 are respectively connected to a plurality of bit lines BL, ... Column selecting transistors 12-1, ..., the gates of which receive column selecting signals Y_0, Y_1, ... Y_n, are respectively connected midway along the plurality of bit lines BL, ... The potentials of the bit lines BL selected by the column selecting transistors 12-1, ... are applied to one input terminal of a sense amplifier 14 through a pass transistor 13-1. Similarly, the transistors formed in the memory cell array 11-2 are respectively connected to a plurality of bit lines $\overline{BL}$ ..., and column selecting transistors 12-2, ..., the gates of which receive the column selecting signals Y_0, Y_1, ..., Y_n, are connected midway along the plurality of bit lines $\overline{BL}$ .... The potentials of the bit lines $\overline{BL}$ selected by the column selecting transistors 12-2, ... are applied to the other input terminal of the sense amplifier 14 through a pass transistor 13-2.

In the EPROM of this embodiment, each memory cell for storing 1-bit data consists of two transistors, and the two transistors are formed to be separated from each other in the different memory cell arrays 11-1 and 11-2. In addition, the bit lines BL, ... are connected to the memory cell array 11-1, and the bit lines $\overline{BL}$ ... are connected to the memory cell array 12-2.

With the above arrangement, unlike a conventional arrangement, the two column selecting transistors 12-1 and 12-2 which receive the same column selecting signal are not adjacent to each other but arranged to be separated by a predetermined distance. Therefore, the bit lines BL, ... and the bit lines $\overline{BL}$ ... do not cross each other. For this reason, the bit lines need not jump by using a diffusion layer or the like, and a wiring pattern can be easily formed. In addition, since a variation in wiring resistance between the bit lines is decreased, symmetry of the column selecting transistors is not degraded.

Fig. 4 is a plan view of a pattern showing an arrangement of a column selecting transistor section (column selector) on the memory cell array 11-1 side in the circuit in Fig. 3. Note that the column selector on the memory cell array 11-2 side is arranged as described above. In Fig. 4, a column selecting signal is a 16-bit signal consisting of bits Y_0, Y_1, ..., Y_{15}, and any one of sixteen bit lines BL, ... is selected by the 16-bit signal. Conductive patterns 21, ... which vertically extend in Fig. 4 serve as the bit lines BL, and the conductive patterns are connected to the memory cell array 11-1 in Fig. 3. Conductive patterns 22 which are formed to cross the conductive patterns 21 are gate wires of the column selecting transistors 12-1 in Fig. 3. In addition, reference numeral 23 denote diffusion regions serving as source

and drain regions of the column selecting transistors, each of the diffusion regions 23 is connected to a corresponding one of the conductive patterns 21 through a predetermined contact hole 24. A conductive pattern 25 located in the center in Fig. 4 is connected to the diffusion regions 23 serving as common source or drain regions through the contact hole 24, and the conductive pattern 25 is connected to one input terminal of the sense amplifier (SA) 14 through the pass transistor 13-1.

Since the column selector with the above arrangement does not have any overlapping pattern but has simple pattern repetition, it can be easily formed. In addition, since the patterns have simple structures, pattern symmetry between the memory cell arrays 11-1 and 11-2 can be easily obtained, and characteristics of elements constituting a memory cell including column selecting transistors can be uniformed.

Fig. 5 is a plan view of a pattern showing an arrangement of the memory cell array 11-1 of the circuit in Fig. 3. As described above, each of memory cells consists of first and second transistors, the first transistors of the memory cells are formed in the memory cell array 11-1. In Fig. 5, a plurality of word lines WL are formed to horizontally cross a plurality of element isolation regions 31. The word lines WL are opposite to each other through the common source regions 32 vertically sandwiched between the element isolation regions 31 in Fig. 5, and the word lines WL are wired such that each pair of word lines WL are set at the same potential. In hatched regions (Fig. 5) which are horizontally sandwiched between the element isolation regions 31, floating gates are formed on the underlayer of the word lines WL. Two non-volatile transistors are staggered in each region. A plurality of bit lines BL are formed to cross the word lines WL, and the bit lines BL are connected through drain contacts 34 to the common drain region 33 for a pair of transistors sandwiched between the element isolation regions 31.

Source lines SL which are connected to the source regions 32 of the transistors through source contacts 35 are formed every N (N is a positive number) bit lines of the plurality of bit lines BL. Note that although each of the source lines SL may be formed every other bit line BL, when a resistance between the source of each transistor and the source line SL can be neglected, each of the source lines SL can be formed every several bit lines as shown in Fig. 5.

Although the memory cell array 11-2 is not shown, the memory cell array 11-2 can be arranged to have the same pattern layout as described above. That is, when impurity ions are implanted in channel regions of two transistors constituting each memory cell to control a threshold voltage, the impurity ions can be implanted in the transistors of the memory cell array 11-1 and 11-2 at the same angle in the same direction. Therefore, characteristics of two transistors of each of the memory cells can be easily uniformed. In addition, since a source line is formed every N (N is a positive number) bit lines $\overline{BL}$, the same pattern layout as shown in Fig. 5 can be obtained. Thus, the source lines SL are formed to have equal intervals in the memory cell arrays 11-1 and 11-2, and distances between the source lines SL and the memory cells can be averaged.

As described above, according to this embodiment, in a memory using differential cells, symmetric memory cell patterns can be obtained in two memory cell arrays. Since a pair of data storing transistors are connected to a sense amplifier through signal lines having the same pattern, a desired layout can be obtained in the differential cells. In addition, since signal lines having different data need not be alternately arranged, pattern formation is simplified, thereby improving symmetry and reliability of the characteristics of the transistors.

According to the above embodiment of the present invention, a memory cell array has been described by taking an interleaved arrangement pattern as an example. However, as shown in Fig. 6, when a normal memory cell array consisting of transistors which are not alternately arranged or a modification thereof is used, the same effect as described above can be expected. The same reference numerals as in Fig. 5 denote the same parts in Fig. 6. That is, Fig. 6 is a plan view of a pattern showing an arrangement of the memory cell array 11-1 in Fig. 3. In Fig. 6, one transistor of each of differential cells is formed in the memory cell array 11-1. A floating gate is formed on the underlayer of the word lines WL in hatched regions between the element isolation regions 31 to form a non-volatile transistor. A plurality of bit lines BL are formed to cross the word lines WL, and the bit lines BL are connected to the common drain region 33 of a pair of transistors located between one element isolation region 31 through a drain contact 34. Each of source lines SL connected to the common source region 32 of the transistors through a source contact 35 is formed every N bit lines (N is a positive number) of the plurality of bit lines BL. In addition, in the memory cell array 11-2 in Fig. 3, the same pattern layout (not shown) as shown in Fig. 6 is used, and each of the source lines SL is formed every N bit lines of the plurality of bit lines $\overline{BL}$.

In the above description, the present invention is applied to an EPROM having two memory cell arrays. However, as shown in Fig. 7, each of the two memory cell arrays 11-1 and 11-2 may be divided into a plurality of blocks. In this case, the divided memory cell arrays on the BL side and the divided memory cell arrays on the BL side are paired, and the sense amplifier 14 is arranged for every pair of memory cell arrays.

As described above, according to the present invention, there is provided a non-volatile semiconductor memory device having a layout in which column selecting transistors have a simple pattern layout and characteristics of two transistors constituting a memory cell are equal to each other.

Claims

1. A non-volatile semiconductor memory device in which each memory cell for storing 1-bit data consists of two non-volatile transistors, comprising:

   a first memory cell array (11-1) in which first transistors constituting said memory cells are located on both sides along a common source region (32) in a staggered manner;
   a second memory ceil array (11-2) in which second transistors constituting said memory cells are located on both sides along a common source region (32) in a staggered manner;
   word lines (WL) connected in pairs to said first and second memory cell arrays to sandwich said common source region, and connected to the same potential;
   first bit lines (BL) connected to said first memory cell array;
   second bit lines ($\overline{BL}$) connected to said second memory cell array;
   bit line selecting means for selecting said first and second bit lines; and
   a data sense circuit (14) for comparing signal levels of said first and second bit line selected by said bit line selecting means so as to detect data, wherein
   said first and second memory cell arrays (11-1, 11-2) have a common pattern layout, and physical addresses of memory cells selected by the same address signal are located at identical positions of the first and second memory cells.

2. A device according to claim 1, wherein
   said first and second memory cell arrays (11-1, 11-2) are divided into a plurality of blocks, and said data sense circuit (14) is arranged every pair constituting each of the plurality of blocks of said first and second memory cell arrays.

3. A device according to claim 1, wherein
   a source line (SL) is arranged every N (N is a positive number) bit lines of said first bit lines (BL) in said first memory cell array (11-1), a source line (SL) of a transistor is arranged every N (N is a positive number) bit lines of said second bit lines ($\overline{BL}$) in the second memory cell array (11-2), and said first and second bit lines are arranged every M x N (M = 1, 2, ...) lines with respect to said source lines to obtain a symmetrical layout.

Patentansprüche

1. Ein nichtflüchtiges Halbleiterspeicherbauelement, in dem jede Speicherzelle zum Speichern von 1-Bit-Daten aus zwei nichtflüchtigen Transistoren besteht, umfassend:

   - eine erste Speicherzellanordnung (11-1), in der erste Transistoren, die die Speicherzellen bilden, auf beiden Seiten entlang einer gemeinsamen Quellregion (32) in einer versetzten Weise angeordnet sind;
   - eine zweite Speicherzellanordnung (11-2), in der zweite Transistoren, die die Speicherzellen bilden, auf beiden Seiten entlang einer gemeinsamen Quellregion (32) in einer versetzten Weise angeordnet sind;
   - Wortleitungen (WL), die paarweise mit den ersten und zweiten Speicherzellanordnungen verbunden sind, um die gemeinsame Quellregion von beiden Seiten zu umgeben, und die mit dem gleichen Potential verbunden sind;
   - erste Bitleitungen (BL), die mit der ersten Speicherzellanordnung verbunden sind;
   - zweite Bitleitungen ($\overline{BL}$), die mit der zweiten Speicherzellanordnung verbunden sind;
   - Bitleitungs-Auswahlvorrichtung zur Auswahl der ersten und zweiten Bitleitungen; und
   - einen Datenleseschaltkreis (14) zum Vergleich von Signalpegeln der ersten und zweiten Bitleitung, die von der Bitleitungs-Auswahlvorrichtung ausgewählt wird, um Daten zu erfassen, wobei
   - die ersten und zweiten Speicherzellanordnungen (11-1, 11-2) ein gemeinsames Muster-Layout haben, und physikalische Adressen von Speicherzellen, die von den gleichen Adreßsignalen ausgewählt werden, an identischen Positionen der ersten und zweiten Speicherzellen angebracht sind.

2. Ein Bauelement gemäß Anspruch 1,
   wobei die ersten und zweiten Speicherzellanordnungen (11-1, 11-2) in eine Mehrzahl von Blöcken unterteilt sind, und der Datenleseschaltkreis (14) bei jedem Paar, das jeden der Mehrzahl von Blökken der ersten und zweiten Speicherzellanordnung bildet, angeordnet ist.

3. Ein Bauelement gemäß Anspruch 1,
   wobei eine Quelleitung (SL) alle N (N ist eine positive Zahl) Bitleitungen der ersten Bitleitungen (BL) in der ersten Speicherzellanordnung (11-2) angeordnet ist, eine Quelleitung (SL) eines Transistors alle N (N ist eine positive Zahl) Bitleitungen der zweiten Bitleitungen ($\overline{BL}$) in der zweiten Speicher-

zellanordnung (11-2) angeordnet ist, und wobei erste und zweite Bitleitungen alle M x N (M = 1, 2, ...) Leitungen bezüglich der Quelleitungen angeordnet sind, um ein symmetrisches Layout zu erhalten.

Revendications

1. Dispositif de mémoire à semi-conducteur non volatile dans lequel chaque cellule de mémoire pour mémoriser une donnée de 1 binaire est constituée de deux transistors non volatils, comprenant :

   un premier groupement de cellules de mémoire (11-1) dans lequel des premiers transistors constituant lesdites cellules de mémoires sont situés, d'une manière étagée, de chaque côté le long d'une zone de source commune (32) ;
   un second groupement de cellules de mémoire (11-2) dans lequel des seconds transistors constituant lesdites cellules de mémoire sont situés, d'une manière étagée, de chaque côté le long d'une zone de source commune (32) ;
   des lignes de mot (WL) connectées en paires auxdits premier et second groupements de cellules pour prendre en sandwich ladite zone de source commune, et connectées au même potentiel ;
   des premières lignes de binaire (BL) connectées audit premier groupement de cellules de mémoire ;
   des secondes lignes de binaire ($\overline{BL}$) connectées audit second groupement de cellules de mémoire ;
   un moyen de sélection de lignes de binaire pour sélectionner lesdites premières et secondes lignes de binaire ; et
   un circuit de lecture de donnée (14) destiné à comparer des niveaux de signal desdites première et seconde lignes de binaire sélectionnées par ledit moyen de sélection de lignes de binaire de façon à détecter une donnée, dans lequel :
   lesdits premier et second groupements de cellules de mémoire (11-1, 11-2) ont un plan de motif commun, et dans lequel les adresses physiques des cellules de mémoire sélectionnées par le même signal d'adresse sont situées dans des positions identiques de première et seconde cellules de mémoire.

2. Dispositif selon la revendication 1, dans lequel lesdits premier et second groupements de cellules de mémoire (11-1, 11-2) sont divisés en plusieurs blocs, et ledit circuit de lecture de donnée (14) est disposé toutes les paires constituant chacun de la pluralité de blocs desdits premier et second groupements de cellules de mémoire.

3. Dispositif selon la revendication 1, dans lequel une ligne de source (SL) est agencée toutes les N (N est un nombre positif) lignes de binaire desdites premières lignes de binaire (BL) dans ledit premier groupement de cellules de mémoire (11-1), dans lequel une ligne de source (SL) d'un transistor est disposée toutes les N (N est un nombre positif) lignes de binaire desdites secondes lignes de binaire ($\overline{BL}$) dans le second groupement de cellules de mémoire (11-2), et dans lequel lesdites premières et secondes lignes de binaire sont disposées toutes les M x N (M = 1, 2, ...) lignes par rapport auxdites lignes de source pour obtenir un plan symétrique.

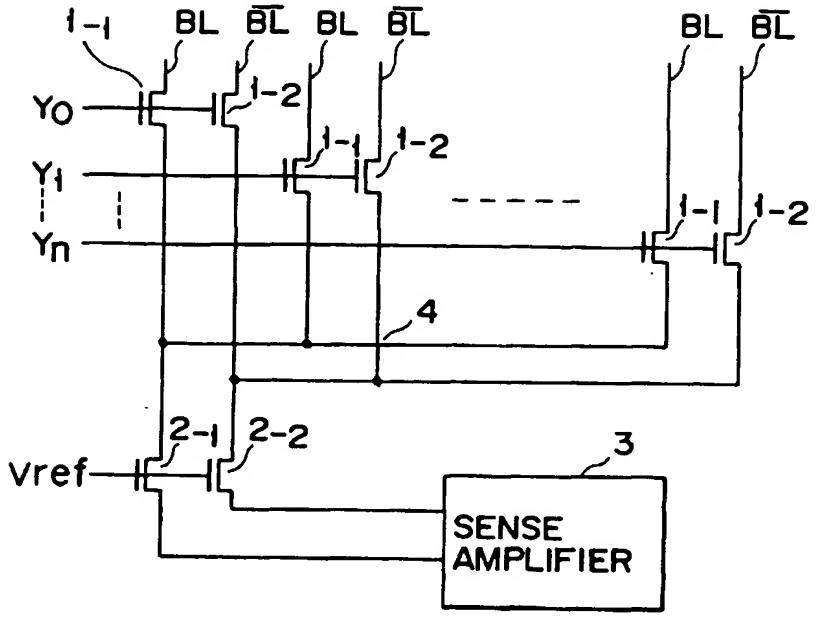


FIG. 1

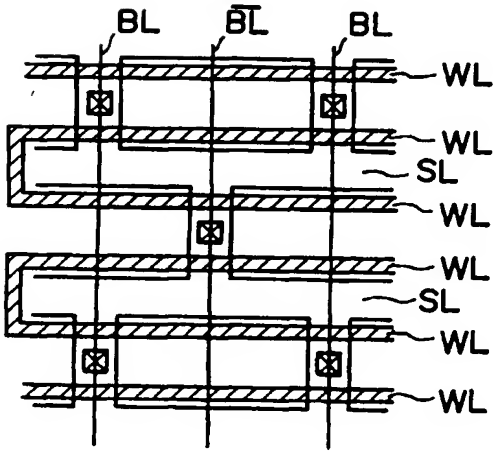


FIG. 2A

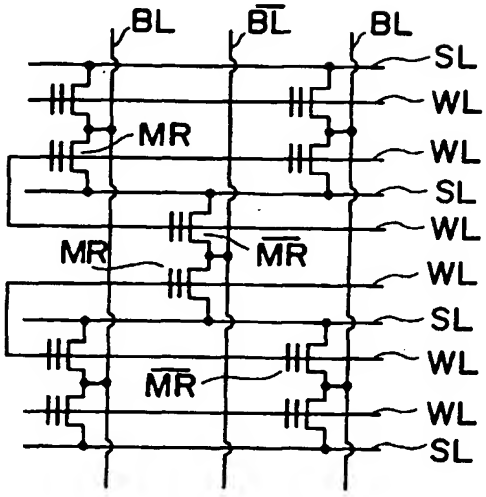


FIG. 2B

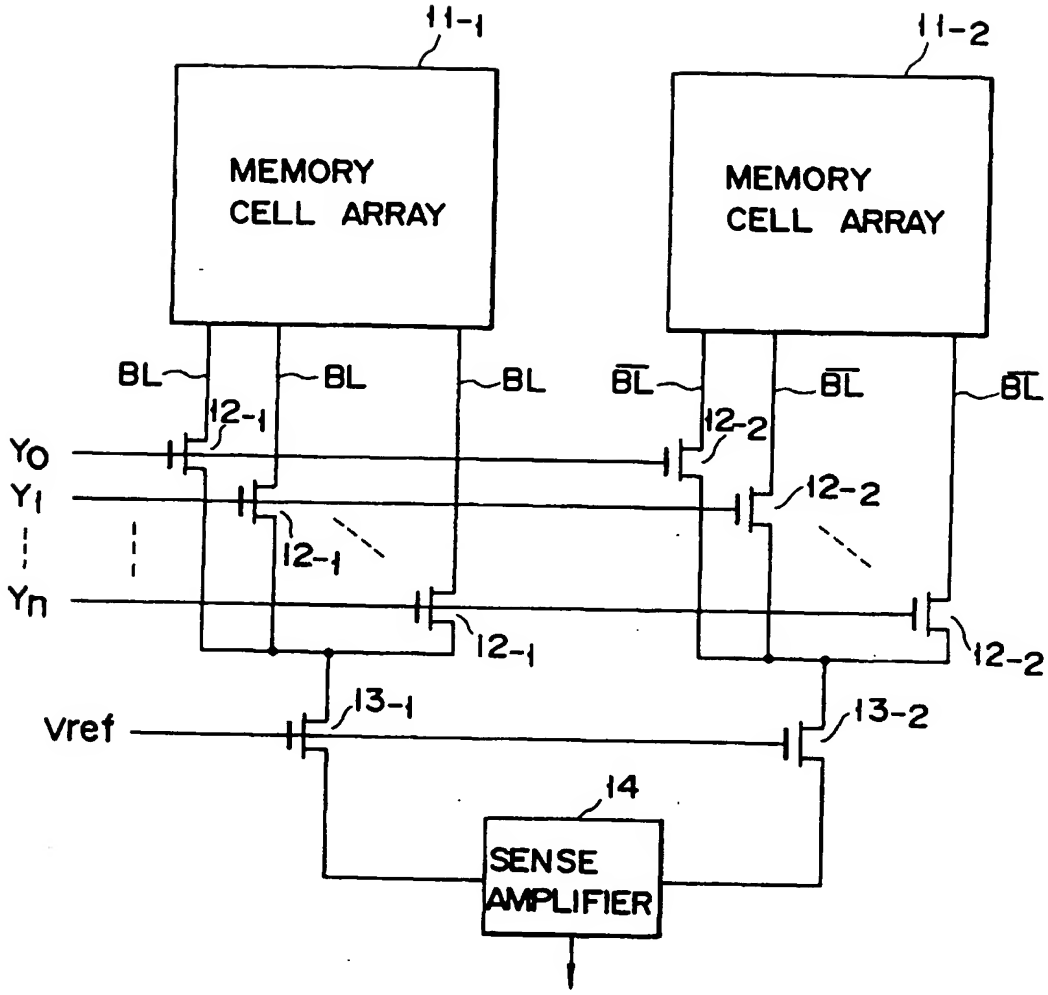

11-1
11-2
MEMORY CELL ARRAY
MEMORY CELL ARRAY
BL
BL
BL
$\overline{BL}$
$\overline{BL}$
$\overline{BL}$
12-1
12-2
Yo
Y1
Yn
12-1
12-2
12-2
12-1
13-1
13-2
Vref
14
SENSE AMPLIFIER

FIG. 3

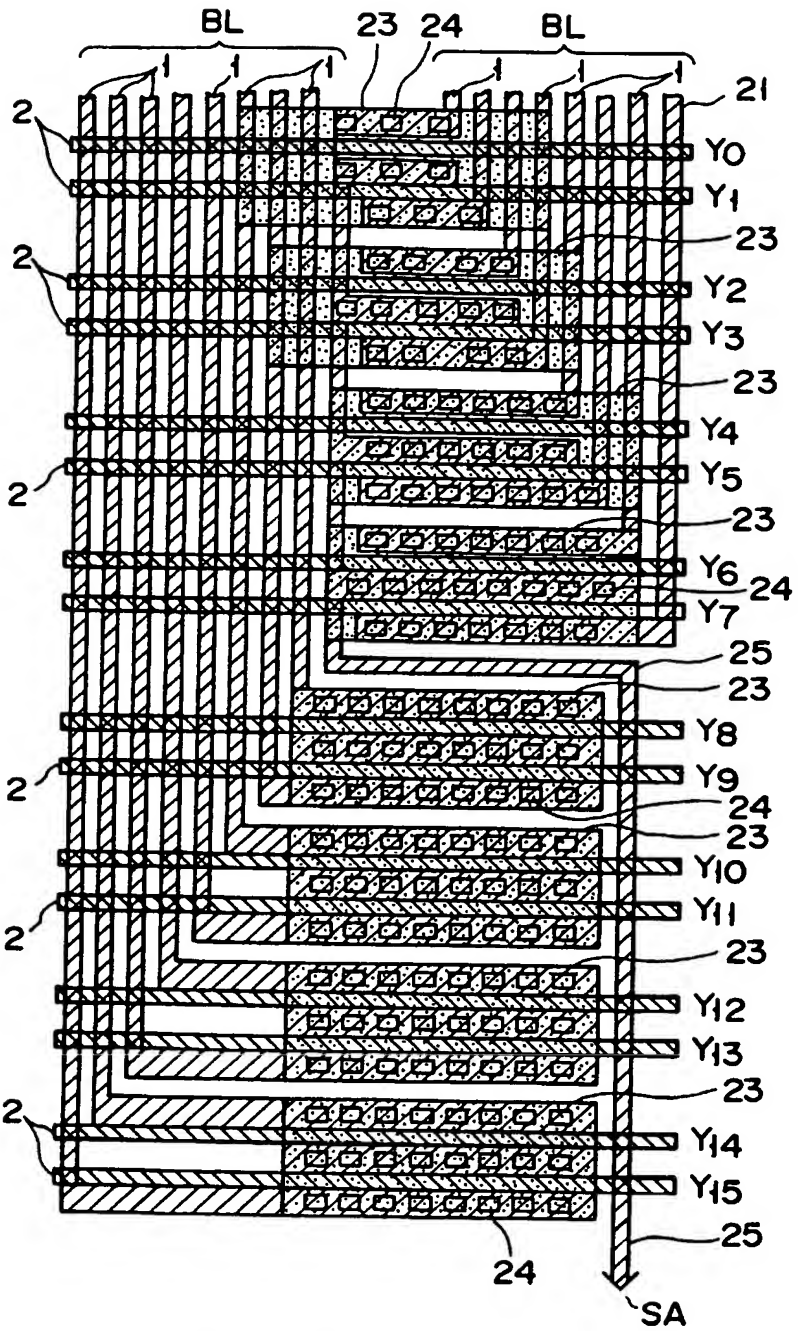
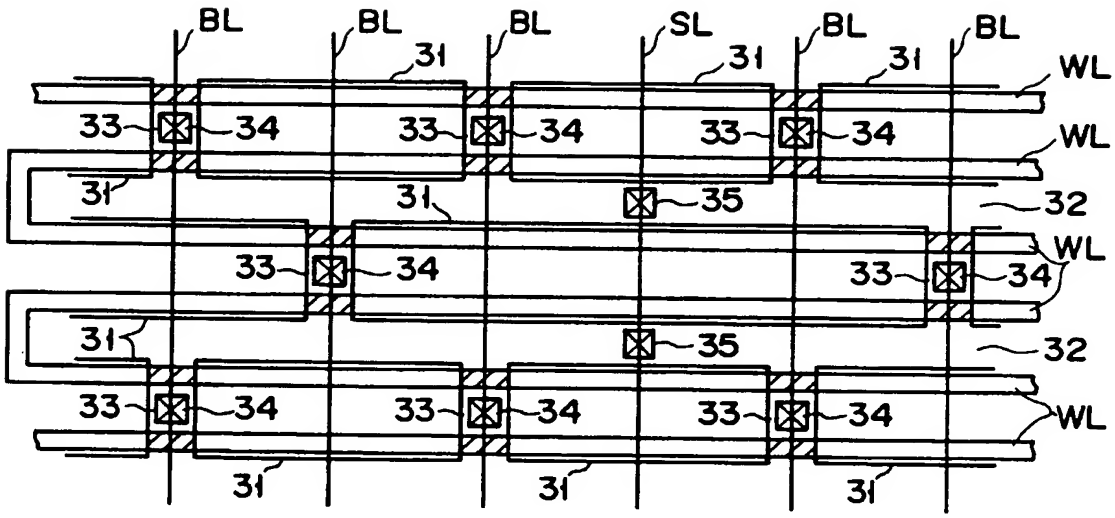

BL
23
24
BL
1
2
21
Y0
Y1
23
Y2
Y3
23
Y4
Y5
23
Y6
24
Y7
25
23
Y8
Y9
24
23
Y10
Y11
23
Y12
Y13
23
Y14
Y15
25
24
SA

FIG. 4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BL
BL
SL
BL
BL
31
31
31
WL
33
34
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34
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WL
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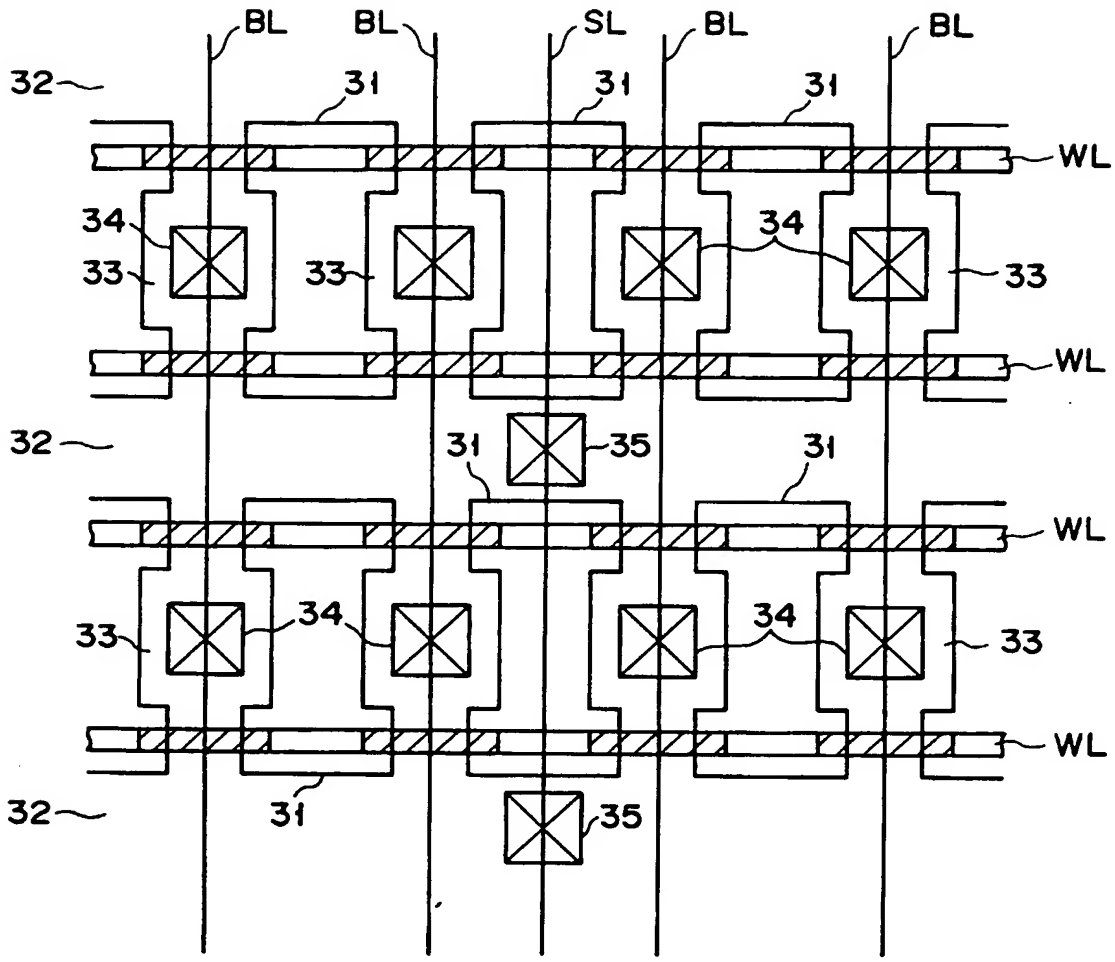
WL
31
31
31

FIG. 5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BL
SL
BL
BL
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WL
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WL
33
34
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33
WL
32
31
35

FIG. 6

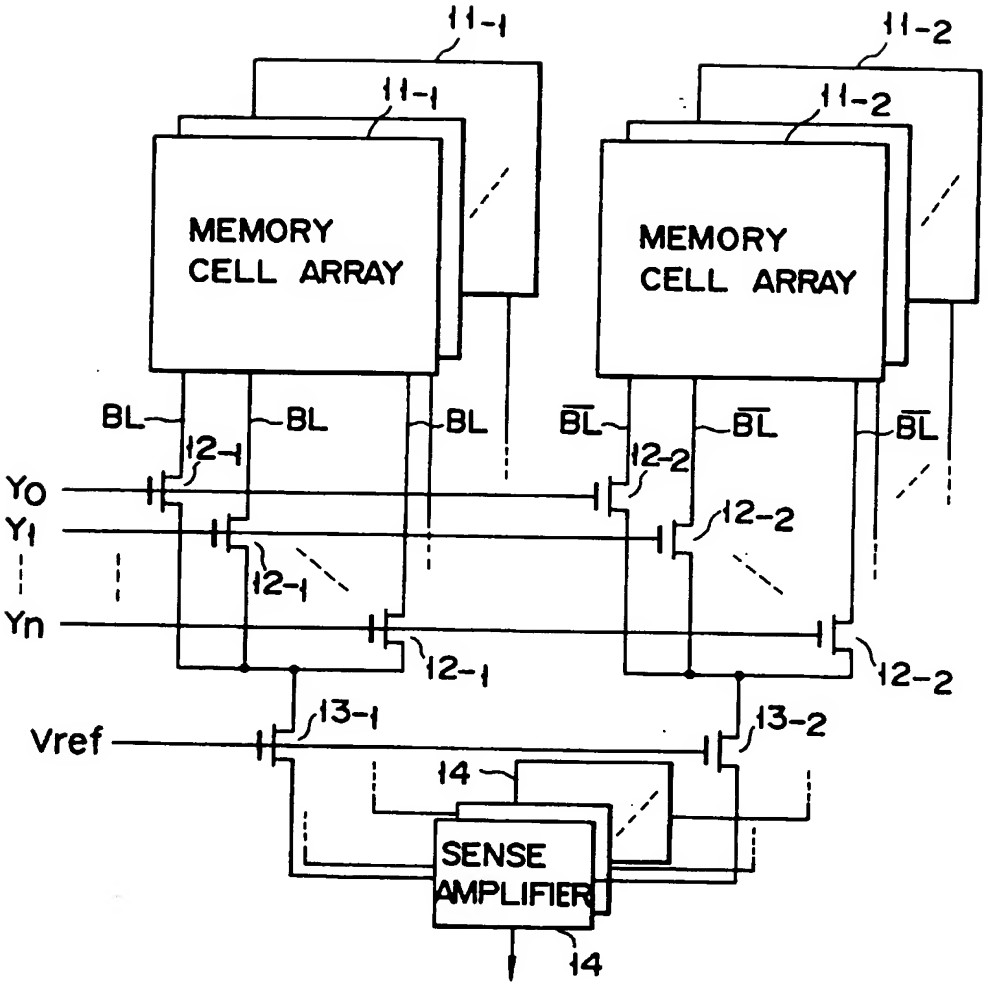
11-1
11-1
MEMORY CELL ARRAY
11-2
11-2
MEMORY CELL ARRAY
BL
BL
BL
BL
BL
BL
12-1
12-2
Yo
Y1
Yn
12-1
12-2
12-2
12-1
13-1
13-2
Vref
14
SENSE AMPLIFIER
14

FIG. 7